The Micro-TO MK II Keyer

BY CHET B. OPAL,* K3CUW

MORE THAN eight years have passed since the Micro-TO Keyer first appeared in *QST*.[1] The design is still basically a good one; however, there have been significant advances in semiconductor technology in the intervening years which make possible a better version of the keyer. The following improvements have been made:

1) Complementary MOS integrated circuits are used, rather than the obsolete RTL ICs and germanium diodes used in the older version. The CMOS circuits operate over a wider voltage range (3 to 15 volts, versus 3.6 volts for the RTL circuits) and draw much less power. Because of the lower power consumption, the new keyer can be battery powered; in fact, the key-up battery drain is so low (less than 1 microampere) that an on-off switch is not even needed.

2) A transistor rather than a reed relay is used to key the transmitter. Since virtually all transmitters now use grid-block keying, it is possible to design the circuit so that a semiconductor replaces the expensive and rather hard-to-find relay.

3) The monitor circuit has been redesigned and is much improved, at the cost of some complication. The new circuit produces a loud, smooth-sounding, clickless and chirpless tone. A monitor volume control has been added.

[1] Opal, "The Micro-TO Keyer," *QST*, August, 1967, p. 17; also *The Radio Amateur's Handbook*, 1969 through 1972 editions.

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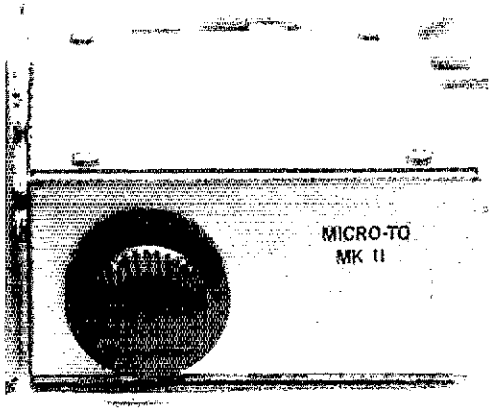


The new keyer handles just like the old one. The logic design is about the simplest which is capable of sending perfect letters. The keyer has no memories, automatic letter spacing, or other frills many of which, in my opinion, one is better off without. One feature it does have is that the clock, which generates the basic timing pulses, is not free running but starts the instant the key is depressed (provided that the mandatory space following the preceding character has been completed). This is particularly an advantage at low sending speeds.

How It Works

The essence of a good keyer is the perfect dot: when the dot side of the paddle is closed, the transmitter should immediately be turned on and it should stay on for a prescribed time (determined by the setting of the speed control), after which it should necessarily remain off for a period exactly as long. A dash should be a sequence of two dots, with the space between filled in.

In the Micro-TO MkII (Fig. 1), dots are formed as follows: normally all inputs to the dot gate (U1A) are at logic "one" (+9 V in this case). Closing either the dot or the dash contact makes one of the inputs a logic "zero" (i.e. ground) and, since this is a NAND gate (which means that if any of the inputs is logic *1*, the output is logic *1*), the output of this gate goes to logic *1*. This triggers the clock, which consists of U2A, U2B, U1B, and U1C. The functioning of the clock is discussed in greater detail below; for the present it is sufficient to know that, once started, it generates one cycle of a square wave. Thus it makes dots, but unfortunately they are not perfect dots (the "mark" is longer or shorter than the "space," depending on the particular unit chosen for U1B, as discussed below). By using additional components it would be possible to trim the clock to form perfect dots, but it is easier to make them by using the dot flip-flop (U4A) to divide the clock frequency by two. Since integrated circuit flip-flops come only in pairs, and since we will need a dash flip-flop later, we may as well use the other half as the dot flip-flop. The flip-flops are type *D* which means that the input at the *D* terminal is transferred to the output *Q* during the positive-going portion of the clock pulse applied to the C terminal. Before the dot started, the *Q* output of U4A was sitting at zero. Thus its complement, $\overline{Q}$, which was applied to the *D* terminal, was a one. When the clock pulse started, its output (connected to the C terminal) transferred this *1* to the output terminal. This *1* in turn

is fed to the output gate, setting its output to ground, which turns on the keying transistor *Q*1.

The keying transistor is a high-voltage pnp type; its purpose is to ground the key terminal (which in a grid-block keyed transmitter lies at −100 volts or so). On key-down the key terminal is clamped to about +0.7 volts by diode CR1. The value of R9 was picked so that a keying current of up to −4 mA can be drawn. If your transmitter draws more than this, R9 can be reduced in value. On the other hand, if your transmitter draws considerably less than this, the value of R9 should be increased because, aside from the monitor transistor, *Q*2, this is the major source of battery drain in the keyer.

Dots are self-completing because, besides keying the transmitter, the output of U2D connects back to the dot gate. Therefore, as the output gate goes to *0* at the beginning of a dot or dash, it grounds pin 8 of U1A so that, so far as the output of U1A is concerned, it appears that the paddle contact is still closed even if it is released. Since pin 8 stays at ground through the end of the character, it forces the clock to generate another square wave. This changes the state of U4A to a zero (because *Q*

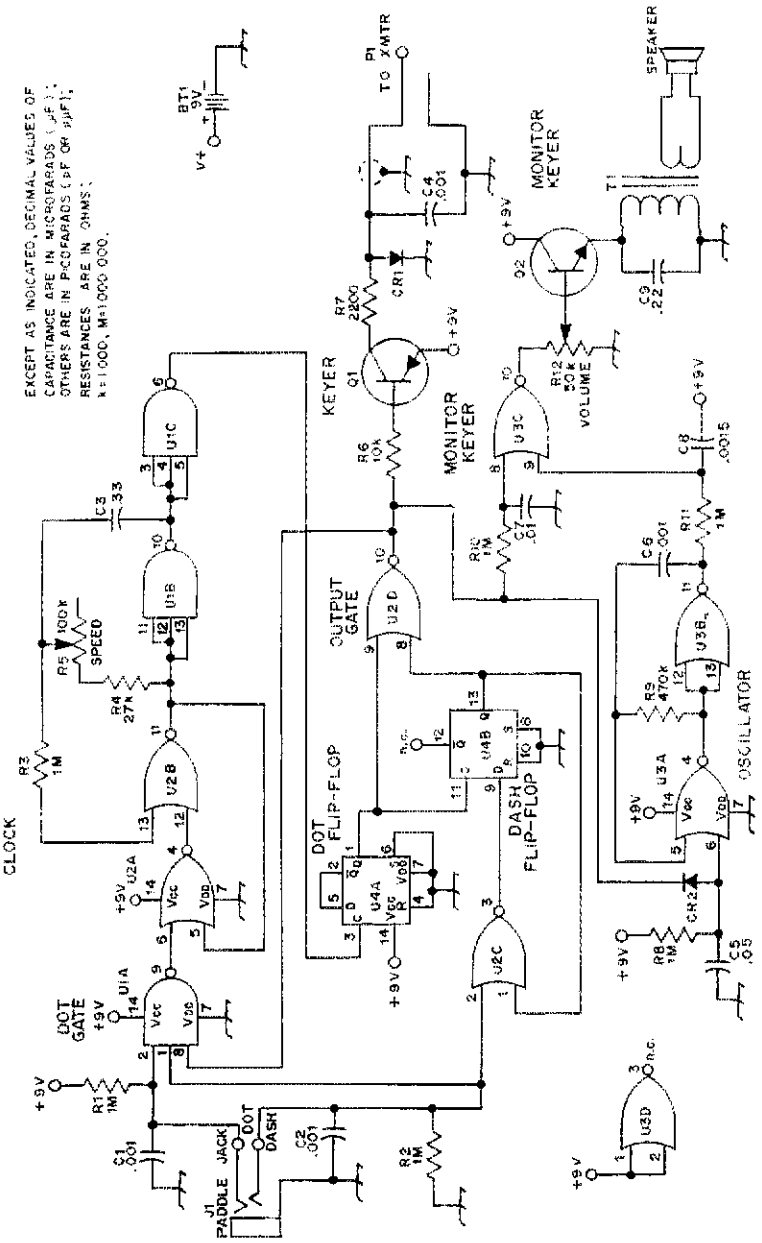
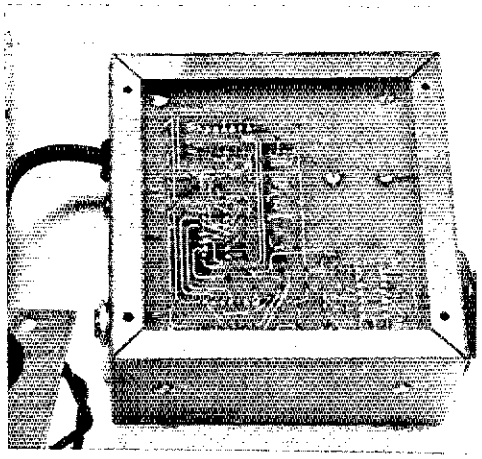


Fig. 1 — Schematic diagram of the Micro-TO Mk II keyer. Since current drain is very low, no on/off switch is included in the unit. The monitor and the keyer are housed in two different chassis boxes. One box could be used if the builder wishes.

BT1 — 9-volt transistor radio battery.
C3 — 0.33-μF mylar capacitor.
CR1 — 200 PIV silicon rectifier (1N4002 or similar).
Q1 — High-voltage pnp silicon transistor (MM4002 2N5415 or similar).
Q2 — General-purpose npn silicon transistor.
R5 — Linear taper, 2-watt carbon.
R12 — Audio taper, 2-watt carbon.
T1 — Audio transformer, 500-ohm primary.
U1 — Triple 3-input NAND gate (CD4023AE, McM4023 or equivalent).
U2, U3 — Quad 2-input NOR gate (CD4001 AE, McM4001 or equivalent).
U4 — Dual type *D* flip-flop (CD4013AE, McM4013 or equivalent).



and hence the *D* input are now *0*), producing a one at the input of U2D. This ends the dot and sets pin 8 of U1A to one. Since all the inputs to the dot gate U1A are now 1, its output goes to *0* and it tries to turn off the clock. But the clock, for reasons described below, is oblivious to this and goes on to complete the second cycle of the square wave, making the perfect space after the perfect dot. It is impossible to start a new character until this space has been completed.

The dash contact of the paddle also goes to an input of U1A, so that closing the dash side of the paddle also starts a dot as described above. But the dash contact is also connected to U2C, a NOR gate. This gate normally has pin 1 sitting at ground, so as the other input goes to ground its output goes to *1*. This *1* is applied to the *D* input of U4B, so as the flip-flop changes state its output (which is connected to the *C* input of the dash flip-flop) causes this *1* to be transferred to the output of U4B. Now both inputs of the output gate U2D are

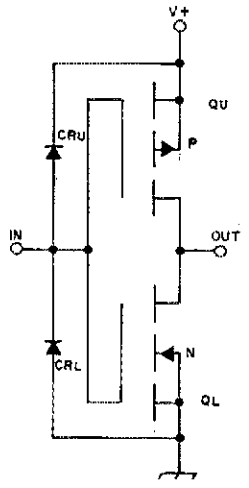


Fig. 2 -- Simplified schematic of an MOS device. See text for a brief description of the operation of the circuit.

one, so its output stays *0*, and hence the transmitter remains keyed, until both U4A and U4B return to *0*. Meanwhile when the *Q* output of U4B, which is connected to an input of the gate U2C, went to one, the output of U2C was forced to go to *0*. But since the output of the output gate is still *0*, the clock pulse will remain present at the input of U1A. Thus a second dot is formed. This time, at the onset of the clock pulse formed when U4A changes back to a *1* at the beginning of the second dot, the *D* input to U4B is at *0*. Thus the output of U4B goes to *0*, and finally when U4A goes to *0* at the end of the second dot, all the inputs to the output gate are at *0* and its output at last goes back up to *1*, ending the dash. Meanwhile, the clock has been forced to start a fourth and final square wave, ensuring that the appropriate space follows the dash.

So far, nothing has been said which would not apply to any type of logic circuit. In order to understand the functioning of the clock and monitor circuits, however, it is necessary to discuss how CMOS circuits work. The discussion here will be very cursory; the reader is referred to the RCA COS/MOS Integrated Circuits Manual for details. The basic CMOS circuit (an inverter) is illustrated, in a simplified manner in Fig. 2. It consists of a p-channel MOS transistor in series with an n-channel MOS transistor and a pair of protective diodes, CRU and CRL (the latter are important in the operation of the clock circuit). When the input is grounded, the gate of the p-channel transistor (QU) sees a voltage which encourages it to conduct, and the n-channel transistor (QL) is cut off. Thus the output circuit is clamped to V+. When the input goes to full positive voltage (V+), the opposite happens and the output is clamped to ground. Since the gate circuits draw negligible current and the diodes never conduct, the circuit draws essentially no power in the quiescent state. And because the voltages at which the gates cause the transistors to conduct are chosen so that they never both conduct at the same time, the only power drawn by the circuit is that used to charge and discharge stray capacitance. A NOR gate is made by hooking up a number of such pairs with all their QLs in parallel and their QUs in series; a NAND gate is made conversely. A type *D* flip-flop is much more complicated and will not be discussed here.

The basic clock consists of gates U2A, U2B, and U1B. Gate U1C is an inverter, which generates clock pulses of the proper polarity to feed the dot flip-flop.[2] Normally, the output of dot gate U1A is at ground, that of U2A at V+, that of U2B at ground, and that of U1B at V+. At the beginning

[2] It might seem that this gate is redundant, since pulses of the proper polarity are present at the output of U2B. However, the waveform at that output is very soft, and during the positive portions of the clock pulse it is possible for the dot flip-flop to be triggered before U1B changes state. A change of state then rushes through the output gate, dot gate, and clock gates, turning off U2B before it has a chance to turn off U1B. The result, for certain combinations of integrated circuits, is that the characters are not completed. Naturally, this was discovered the hard way.

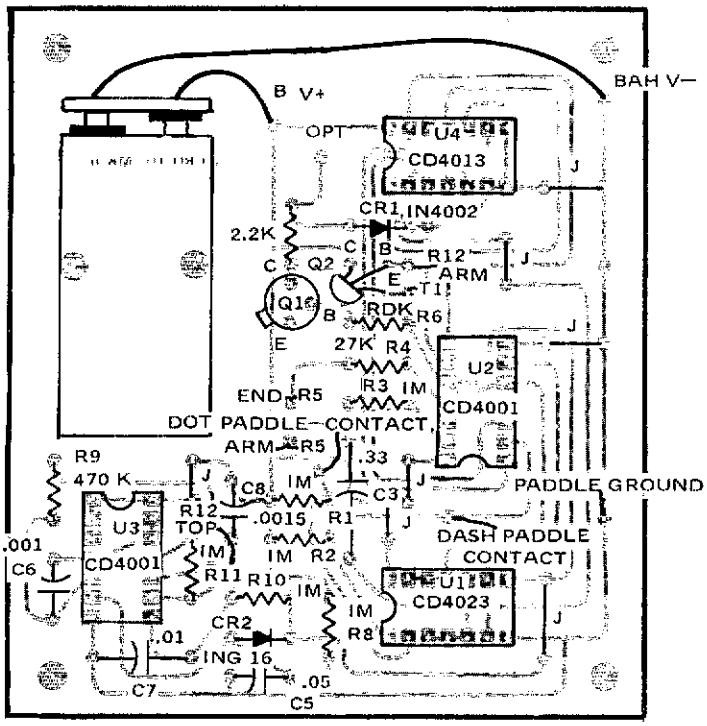


Fig. 3 — Scale drawing of etching pattern from component side of board showing component placement. J = wire jumper.

of a character, U1A goes to V+, forcing the output of gate U2A to ground. This feeds a *0* to one input of NOR gate U2B, and since the other input is also at *0*, the output of U2B goes to *1*, forcing the output of U1B to ground. Now capacitor C3 has been sitting with V+ at the terminal connected to the output of U1B and the other side at ground. Consequently, as the side connected to U1B went to ground, a more negative voltage appeared on the other side. A large-value resistor, R5, is installed in series with pin 13 of U2B so that this voltage is not shorted to ground by the protective diodes on that pin. The main discharge path for C3 is then through R4 and the speed control, R5, to the output of U2B, which is sitting at V+. As that terminal of C3 heads for V+, it eventually puts a *1* at pin 13 of U2B. At that time the output of U2B goes to *0*, the output of U1B goes to *1*, and that side of C3 goes to V+. The other side of C3 now goes to nearly twice V+. Again, C3 discharges through R4 and R5 to the voltage at the output of U2B, which is now ground. As C3 heads to ground, it eventually puts a *0* at pin 13 of U2B, the output of U2B goes to *1*, and the whole cycle repeats. Thus, so long as pin 12 of U2B is at ground, the clock will oscillate. Pin 12 is kept at ground via the dot gate U2A whenever the mark portion of a character is being generated. In addition, the other input to U2A comes from U2B itself, so that if a clock cycle is started it must continue until the output of U2B goes to *0*. This happens during the second half of the clock cycle, which continues no matter what the input at pin 12 of U2B is. Thus a clock cycle, once started, is self-completing. Since all inputs to the dot gate cannot go to *0* at the end of a character until a clock cycle has been started, the completion of that clock cycle inserts an automatic space at the end of the character, as desired.

The frequency of oscillation of the clock, and hence the keying speed, is independent of supply voltage, since the voltage swing across C3 is proportional to supply voltage and the voltages at which U2B changes state are also proportional to supply voltage. The clock output is not a symmetrical square wave, however, because voltages corresponding to a *1* and a *0* at the input of U2B are not symmetrical; that is, for a supply voltage of 9 V, U2B may be turned off at +2 V and on at +5 V, so that as the clock oscillates C3 discharges through +11 V in one direction and −13 V in the other. The keying speed range is determined by the combination of R4, R5, and C3. The values selected give a range of 12 to 60 wpm.

Construction

The complete keyer is housed in a 3 × 4 × 5-inch utility cabinet, and the unit less monitor fits easily into a 2 × 4 × 4-inch cabinet (see illustrations). The prototype was built on Vector type 59P44/032 board, which is drilled on 0.1-inch centers. Hard wiring between sockets and flea clips was used, but these are unnecessary (the sockets were used for testing different type ICs, and the flea clips represented terminals for designing a printed circuit board). Later a printed circuit board was made; this is shown in Fig. 3. The pc-board layout can be used as a guide for a hard-wired circuit if desired. Nearly all components are on the

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Semiconductors

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Hookup and Adjustment

Disconnect the cable which runs from the output of the 2-watt module to the antenna connector. Connect the output of the 10-watt amplifier to the antenna connector, and the output of the 2-watt module to the input of the 10-watt stage using RG-174 or RG-58 cable. Connect a wire from the dc-input terminal on the amplifier board to the +V binding post on the rear apron. Attach a 50-ohm dummy load to the antenna connector and a regulated supply to the appropriate power terminals. The completed transmitter draws approximately 1.1 amperes from the power source. During initial tuneup the output of the transmitter should be monitored with the FET voltmeter and rf probe. Key the transmitter and adjust C24 for maximum output. R 8 on the buffer/amplifier board should be adjusted for a 17.5-volt reading on the voltmeter. This voltage corresponds to 6-watts output power. Spectral analysis revealed that the second harmonic was down 40 dB, and no significant spurious outputs were present anywhere in the spectrum – a clean transmitter indeed! QST

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board. The rf bypass capacitors C1, C2, and C4 are mounted at the points where their leads enter the cabinet. C9 is mounted across the terminals of T1.

The circuit board is mounted with small angle brackets near the top of the enclosure. The speaker is mounted over a pattern of 7/32-inch holes. There are rubber grommets on the bottom plate to keep the keyer from sliding around and to raise it above the table so the sound can be heard; the whole box then acts as an effective baffle, and the down-facing holes do not collect dust. The speed and volume controls are mounted on the narrow end which does not have the seam. The output transformer, jack for the paddle leads, and output lead are on the rear.

Obtaining components in this time of shortages may be difficult. The CMOS integrated circuits are manufactured by RCA, Motorola, Solitron, Solid State Devices, etc. They are specified by Cx400*1yz*, where the *x* indicates the manufacturer, and the *y* and *z* the package type and environmental specs. Any *x*, *y*, and *z* will do. The high-voltage pnp keying transistor may present a problem; examples of RCA and Motorola types are specified. If your transmitter key-up voltage is only −100 V or so, you may be able to select a common 60 V BV$_{ceo}$ transistor to do the job. Any diode will do for CR2; CR1 is a power supply rectifier, since it needs to withstand the key-up voltage. Absolutely any npn silicon transistor will work at Q2. The keyer will run on anything from 3 volts to 15 volts, although it may be necessary to reduce the value of R9 if very low voltages are used. Below about 6 volts, the primary of T1 should have a lower impedance (e.g., about 100 ohms for a 4-V supply) in order to get adequate volume. A complete set of components was priced from the catalog of a single midwestern mailorder house; the keyer with monitor costs $28, complete with an allowance for hardware, wire, and Vectorbord. The version without monitor costs about $9 less.

Two versions of the keyer have been built, one which uses point-to-point wiring and includes the monitor, and another which uses a printed circuit board but has no monitor. The original breadboard unit has been in use at K3GJD for almost two years. The two final versions were used in two recent contests at that station.

I will be happy to correspond with anyone having difficulties with the keyer, or to answer any questions. I will be even happier if, when you write, you will enclose a self-addressed (and perhaps stamped) envelope. Of course, this is largely irrelevant, since everyone's Micro-TO MkII will work perfectly. QST

VHF Converters

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application now in the process of being tried by WA3HMK.

The circuit diagram is drawn in a manner that will illustrate use of feedthrough capacitors as tiepoints and bypasses. All the .001-μF capacitors are small ceramics of the FT type. The 500-pF capacitors are button-micas. Both types are often found as surplus. Each capacitor is shown in the compartment or partition in which it is mounted. All parts shown below the broken line are on the oscillator side of the partition. All above are in the rf portion.

The converter was checked in the ARRL lab and used in communication at WIHDQ. Sensitivity and gain were adequate for weak-signal work. Spurious responses, often a problem in simple converters of the oscillator-multiplier type, were conspicuous by their absence. The value of R1 should be adjusted for a current drain of about 5 mA, or for optimum noise figure. The original is 220 ohms, but higher values may be needed. C1 and the position of the tap on L1 should also be optimized for noise figure. Converter gain can be controlled by varying resistor values in the second stage. – *W1HDQ*

Strays

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